ARITHMETIC STRUCTURES FOR PROGRAMMABLE LOGIC DEVICES

ABSTRACT OF THE DISCLOSURE

According to some embodiments, arithmetic structures in logic elements result from combining inverters and pass gates (or other multiplexing hardware) with LUT hardware. According to other embodiments, arithmetic structures in logic elements result from combining dedicated adder hardware (e.g., including XOR units) and fracturable LUT hardware. According to other embodiments, arithmetic structures in logic elements result from providing complementary input connections between multiplexers and LUT hardware. In this way, the present invention enables the incorporation of arithmetic structures with LUT structures in a number of ways.